IDEC Chip Design Contest

A Double Step-Down Converter with Perturb & Observe MPPT Technique in High-Voltage Energy Harvesting System

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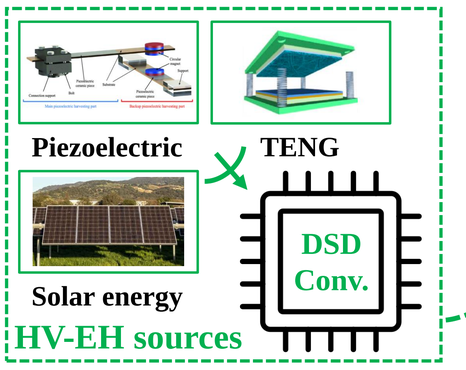
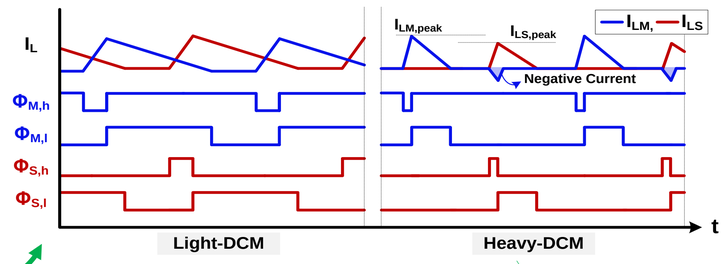
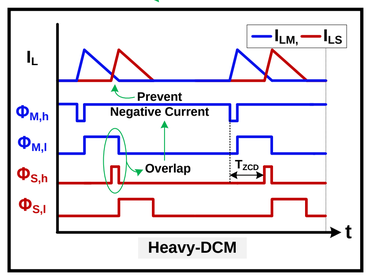
Introduction





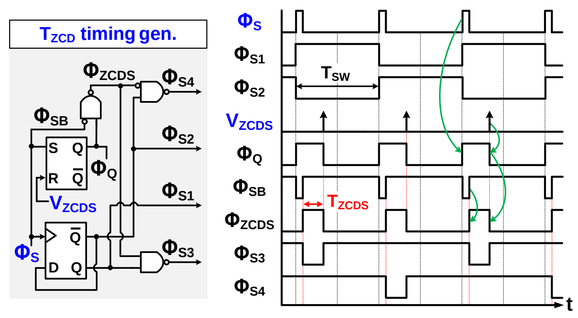
Challenge: Negative I_{LM} → Solution

☹ Increase power loss ☹ V_{CF} offset ☹ I_{LM} & I_{LS} imbalance

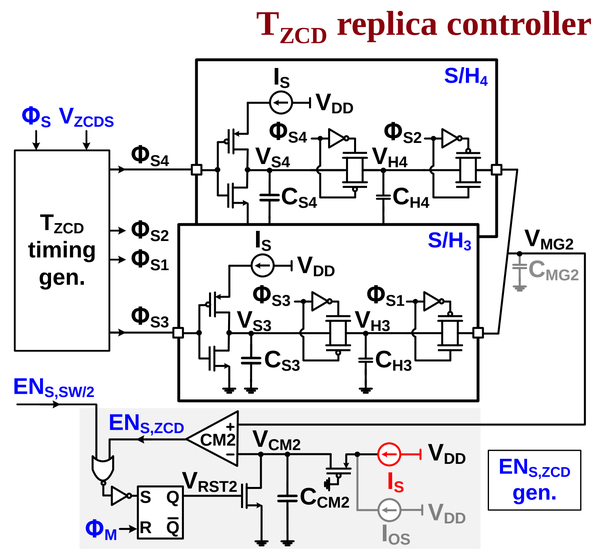


- By intentionally overlapping the conduction intervals of the two phases, the proposed scheme suppresses negative I_{LM} and maintains a continuous charge transfer path through C_F. → T_{ZCD} phase interleaving

Proposed DSD controller

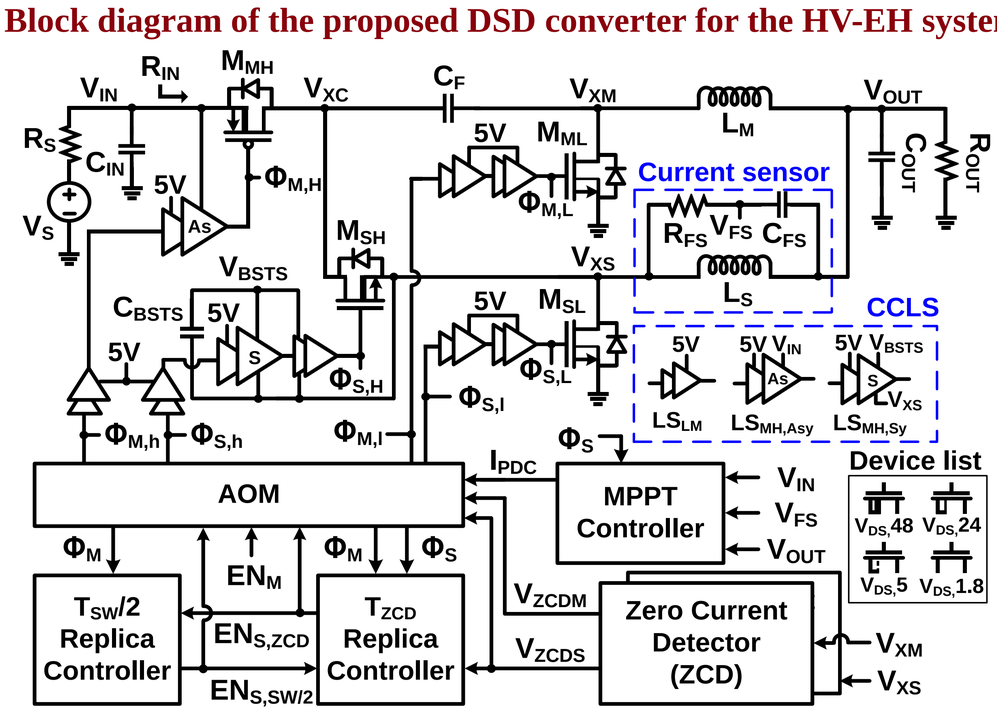


- To prevent negative inductor current, the T_{ZCD} replica controller is proposed.
- The voltage is sampled and held during the T_{ZCD} interval, and based on this stored value, the $EN_{S,ZCD}$ signal delayed by T_{ZCD} is generated.
- T_{ZCDS} is defined as the time interval from the end of Φ_S to the occurrence of V_{ZCDS}.

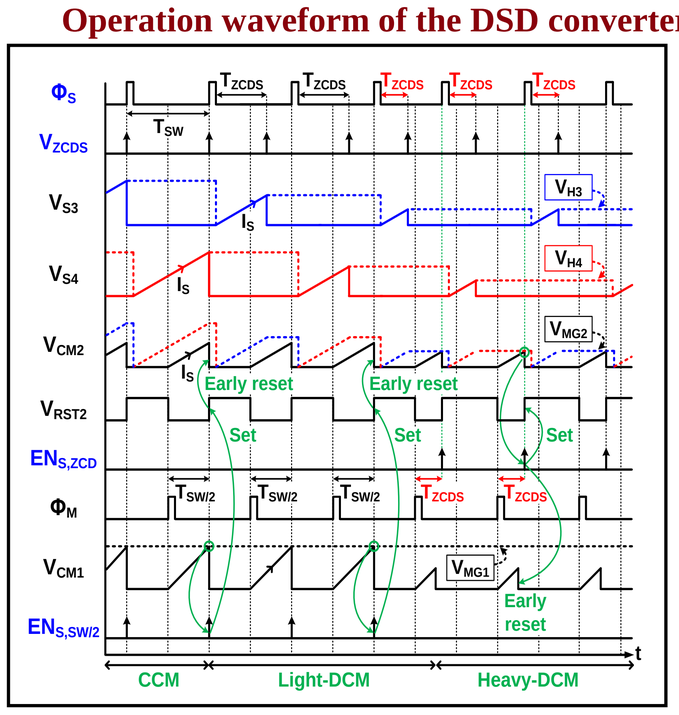


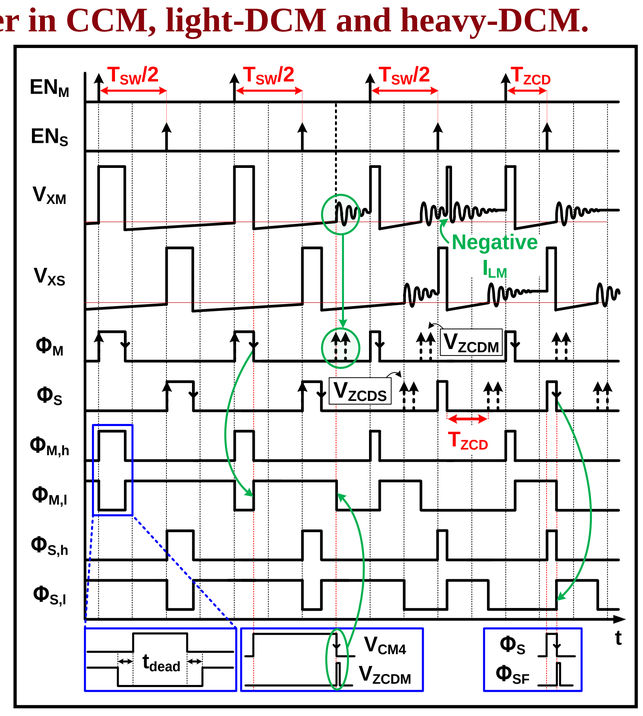
Proposed System Architecture & Operation

Block diagram of the proposed DSD converter for the HV-EH system



Operation waveform of the DSD converter in CCM, light-DCM and heavy-DCM.

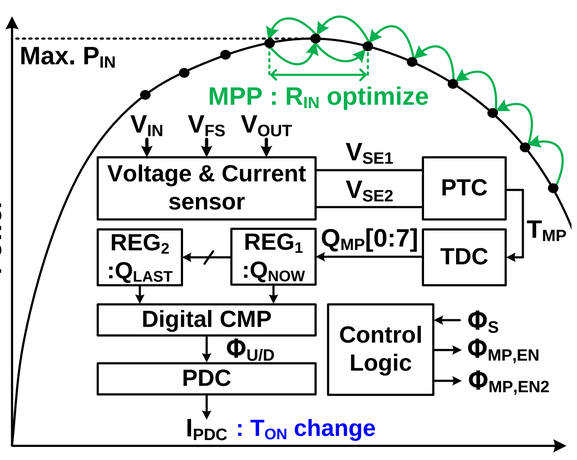




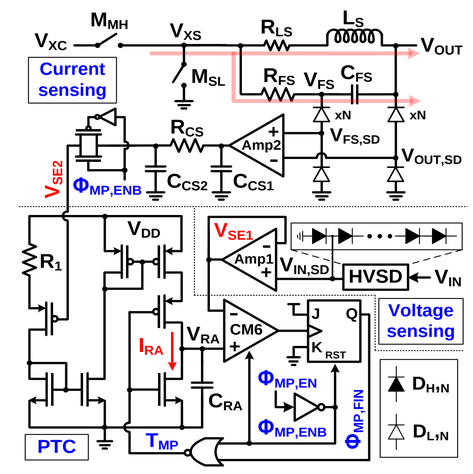
- To reflect the EH source (PV-panel, TENG and PENG) characteristics, the input stage is modeled as a simplified equivalent circuit composed of V_S, R_S, and C_{IN}. The power stage consists of two high-side switches (M_{MH} and M_{SH}) and two low-side switches (M_{ML} and M_{SL}).
- The timing relationship between the master and slave phases is defined by the enable signals $EN_{S,SW/2}$ and $EN_{S,ZCD}$, generated by the $T_{SW}/2$ and the T_{ZCD} replica controller, respectively.
- In the heavy-DCM region, if EN_S is still activated at $T_{SW}/2$, negative I_{LM} can be induced, resulting in an undesired rise of V_{XM}. To avoid this, EN_S is shifted from $T_{SW}/2$ to T_{ZCD} to prevent negative I_{LM}.

Proposed P&O MPPT

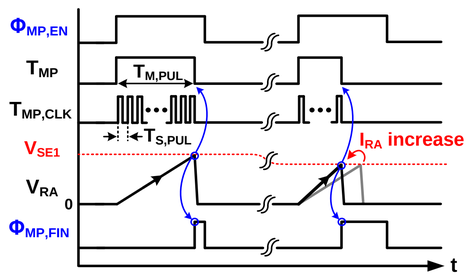
Block diagram of proposed P&O MPPT



PTC with V&I sensors

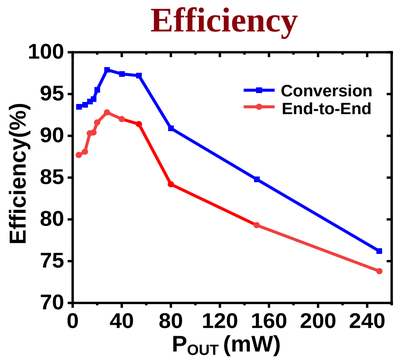


- To optimize the input impedance R_{IN} such that P_{IN} is maximized at the maximum power point (MPP), the MPPT controller compares the present state with the previous state and determines the tracking direction according to the resulting power variation based on the P&O scheme.
- The V&I sensor outputs V_{SE1} and V_{SE2}, which are converted by the PTC into a time-domain signal T_{MP} representing P_{IN}. The TDC converts T_{MP} into $Q_{MP}[0:7]$, which is stored and compared to generate $\Phi_{U/D}$. Based on $\Phi_{U/D}$, the PDC adjusts I_{PDC}, controls T_{ON}, and tunes R_{IN} toward the MPP.

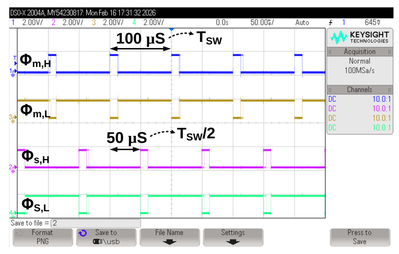


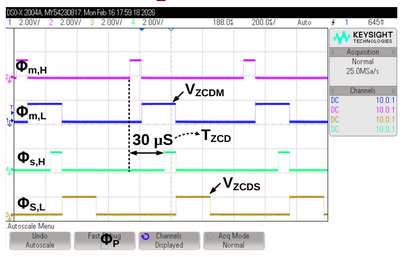
Results

Efficiency

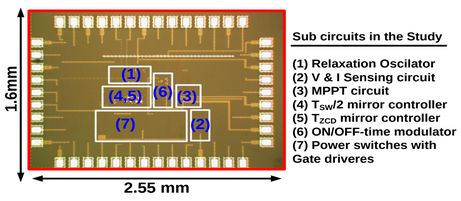


Experiment results



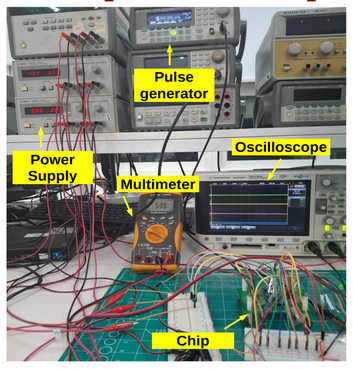


Chip micrograph



Sub circuits in the Study
(1) Relaxation Oscilator
(2) V & I Sensing circuit
(3) MPPT circuit
(4) $T_{SW}/2$ mirror controller
(5) T_{ZCD} mirror controller
(6) ON/OFF-time modulator
(7) Power switches with Gate driveres

Experiment setup



- A HV-EH IC was fabricated in 130nm BCD and its performance was evaluated using the equivalent circuit, model of the EH system.
- In CCM, the $EN_{S,SW/2}$ signal is activated, and the phase difference between Φ_M and Φ_S is defined by $T_{SW}/2$. In contrast, in DCM, the $EN_{S,ZCD}$ signal is activated, and the phase difference between Φ_M and Φ_S is defined by T_{ZCD}.

Conclusion

- By employing the $T_{SW}/2$ and T_{ZCD} replica controllers with AOM, it improves power efficiency in the heavy-DCM region and prevents the negative I_{LM}, thereby avoiding the V_{CF} offset.
- The proposed DSD converter tracks the MPP over a wide range of R_{IN} for HV-EH system.

Acknowledgement

* The chip fabrication and CAD tools were supported by the IDEC (IC Design Education Center).*